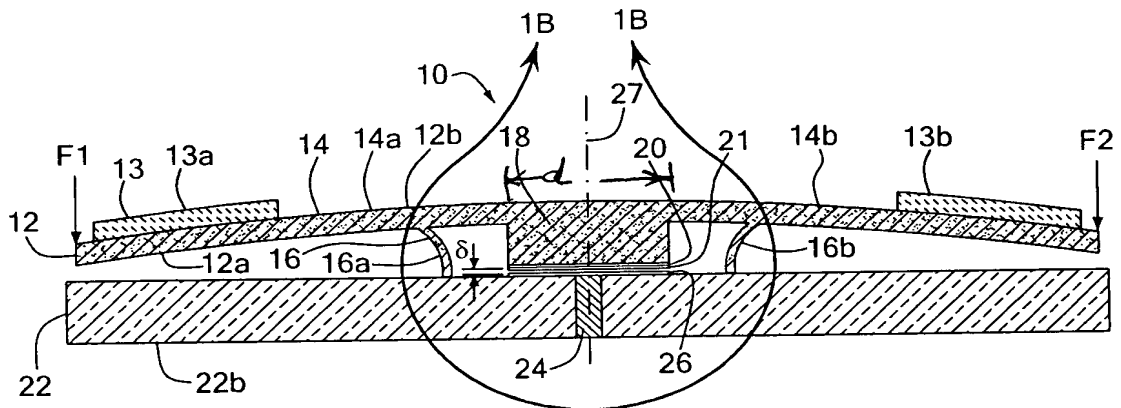


**FIG. 1**



**FIG. 1B**

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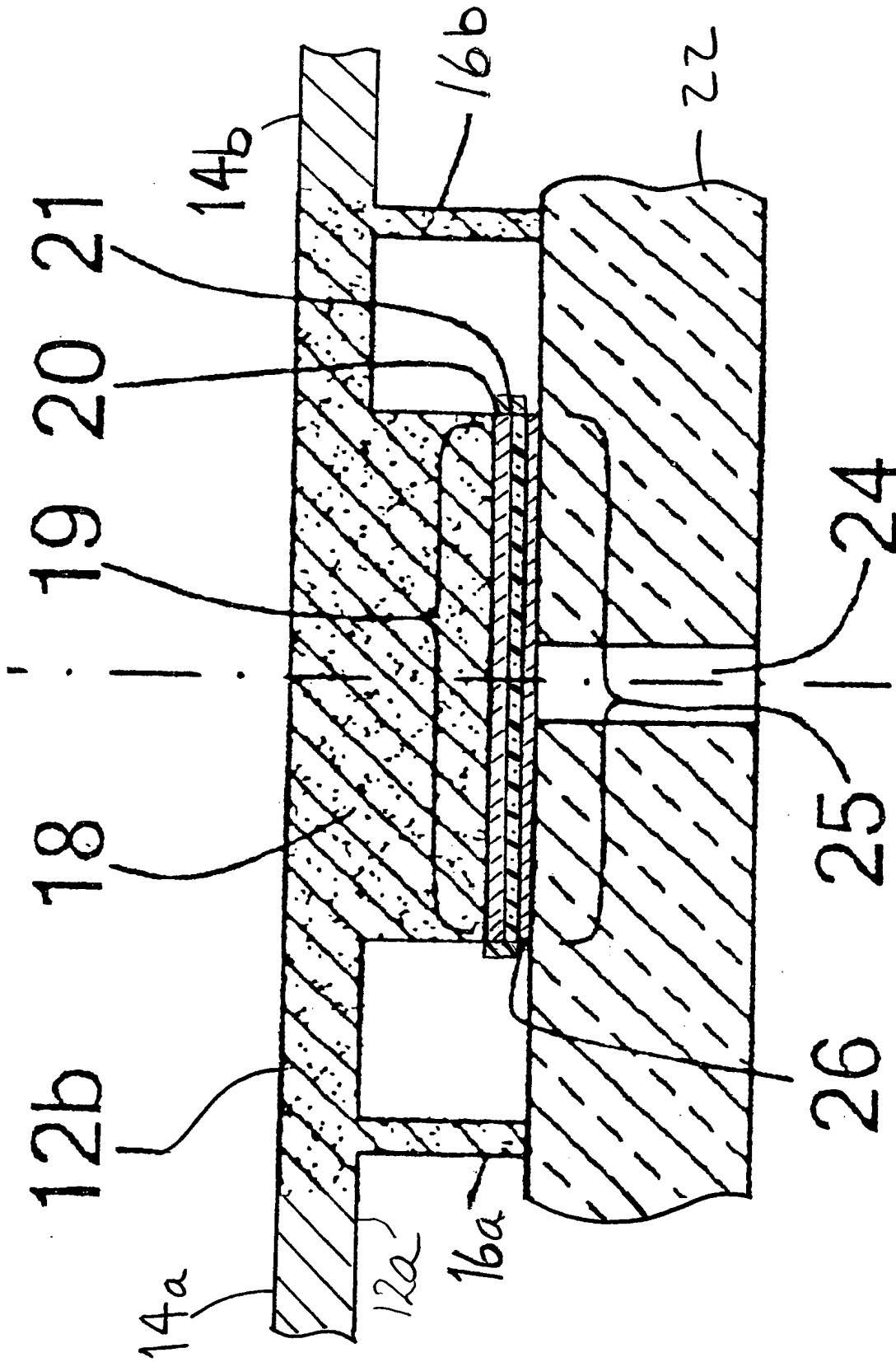
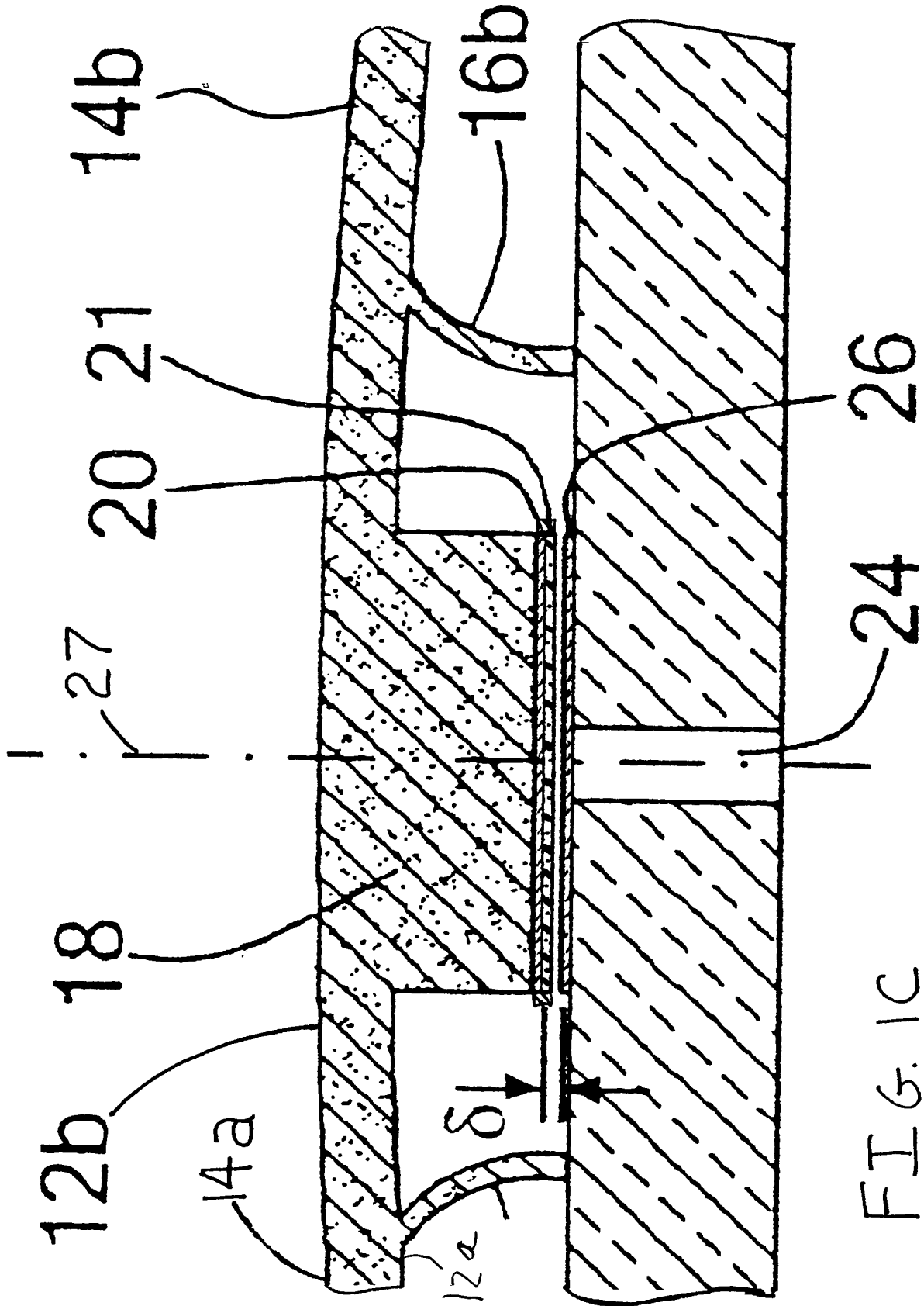
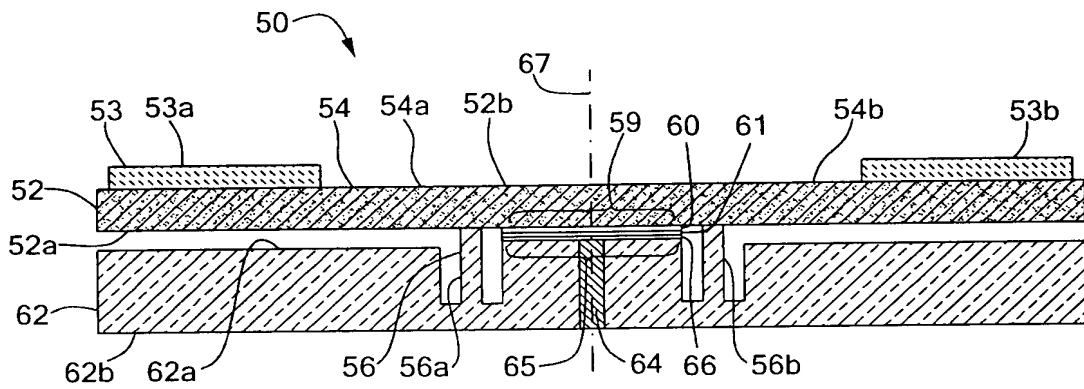


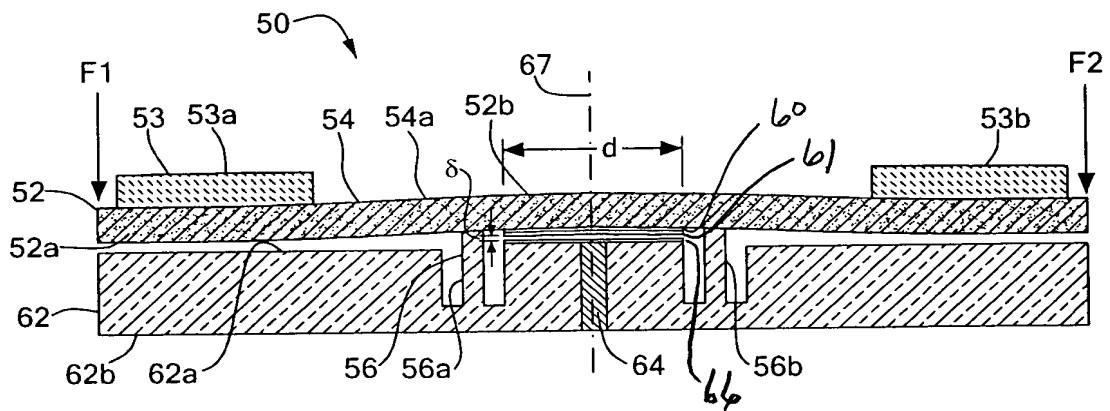
FIG. 1A



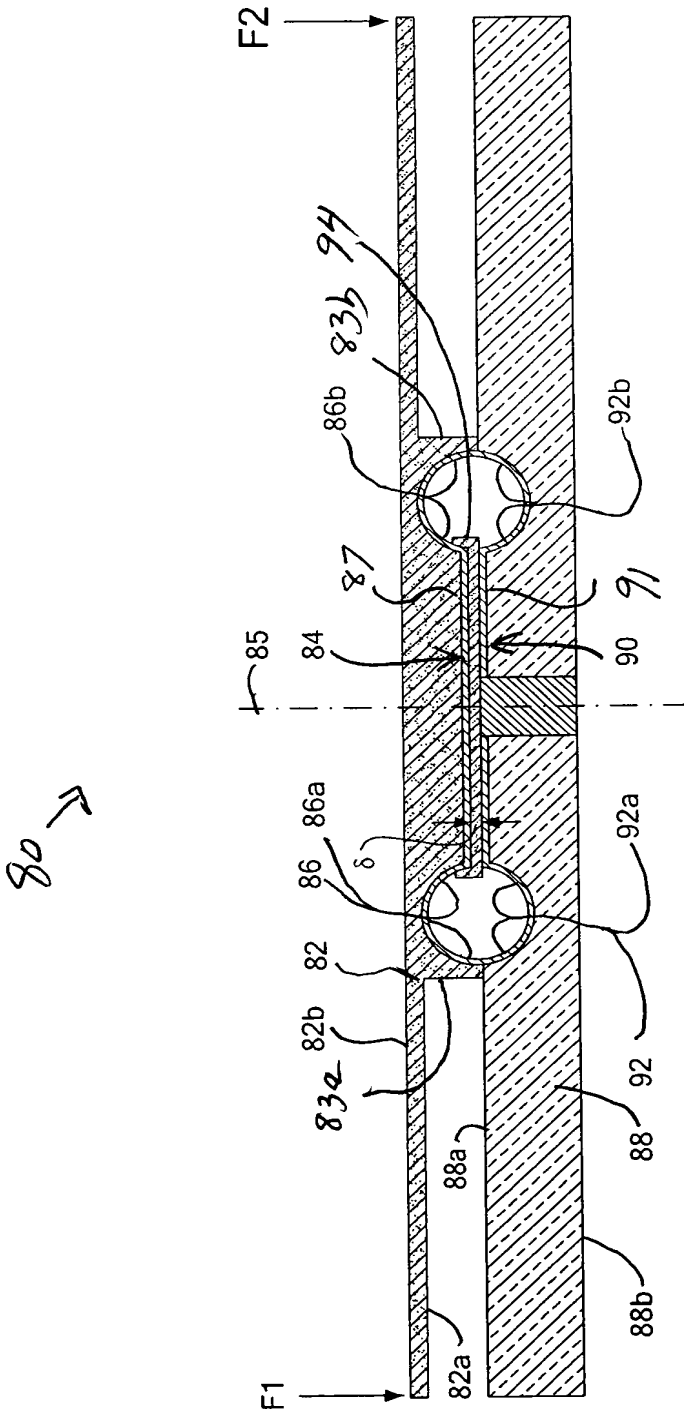
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**FIG. 2**

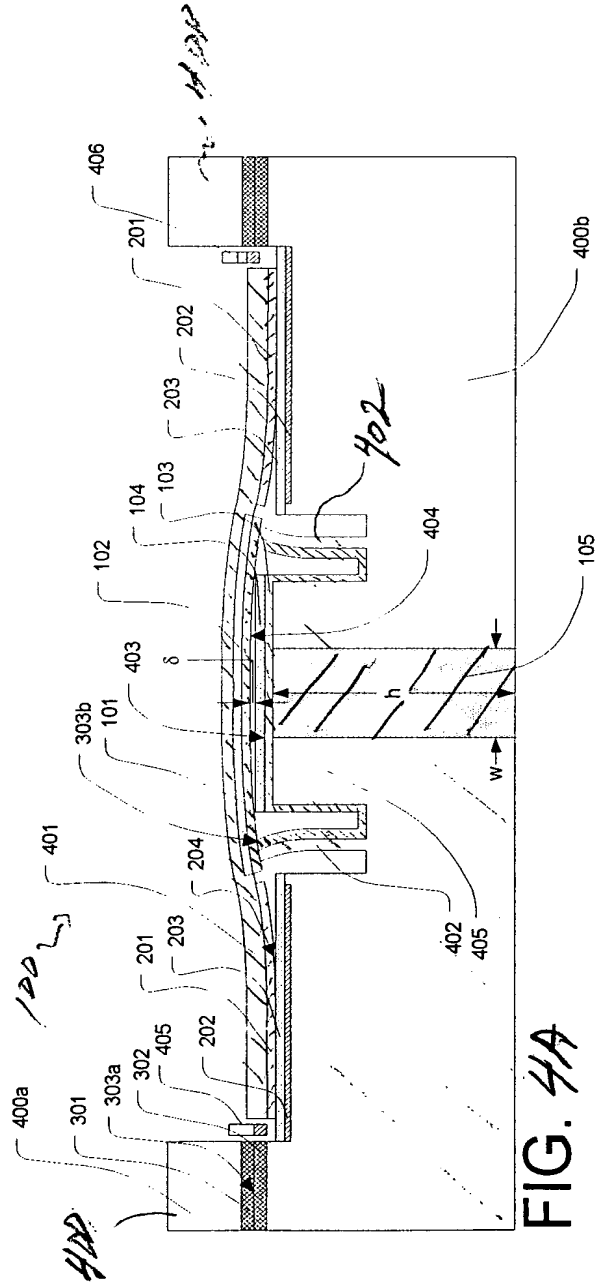
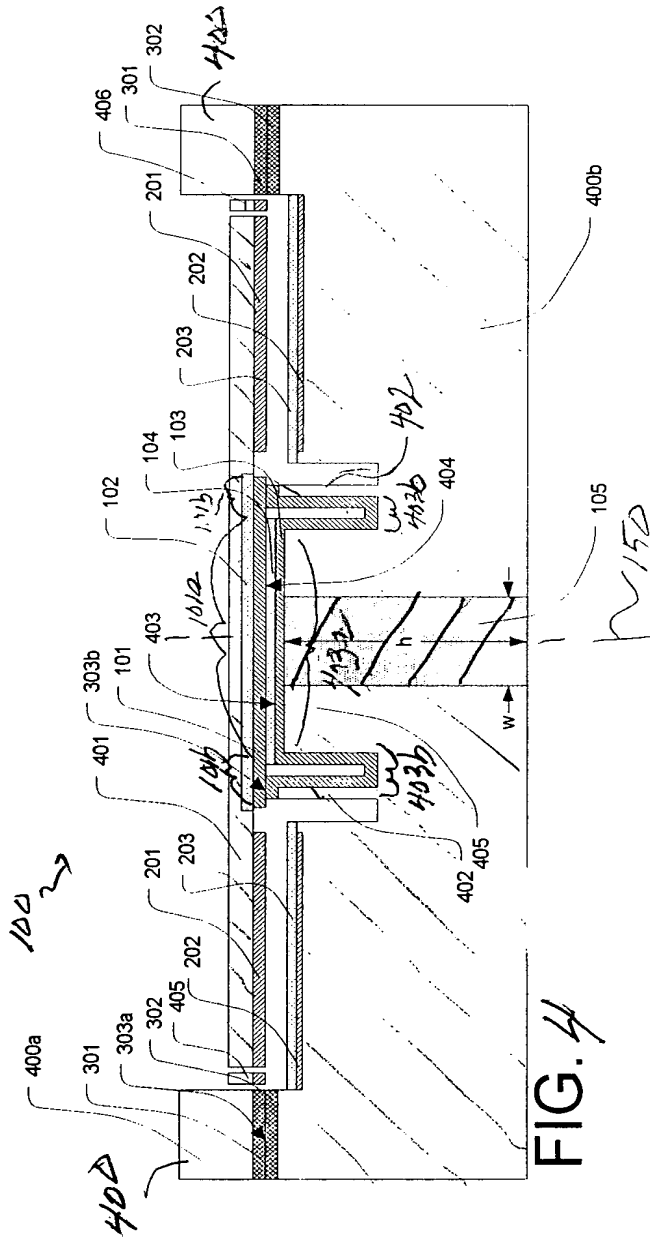


**FIG. 2A**



**FIG. 3**

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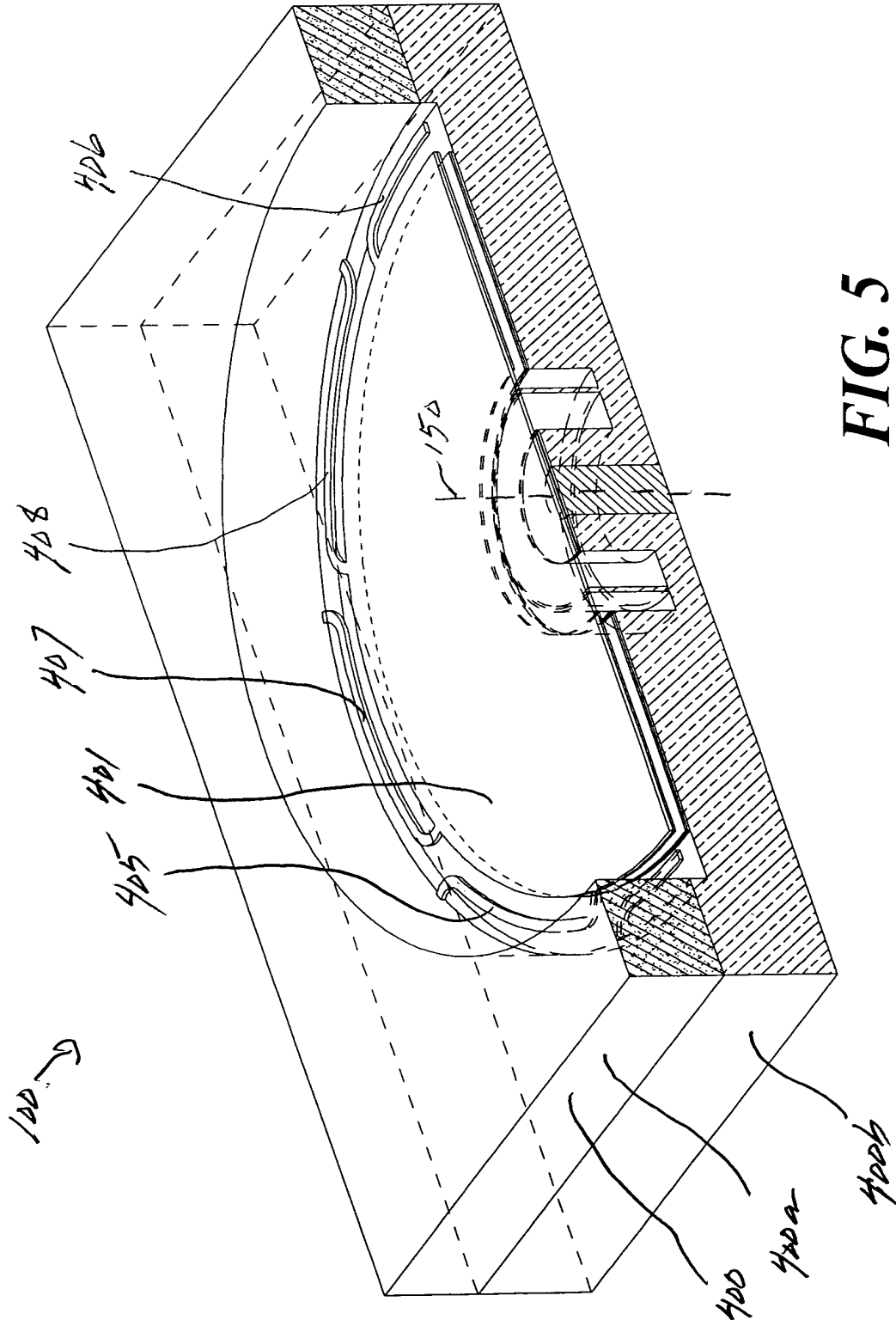
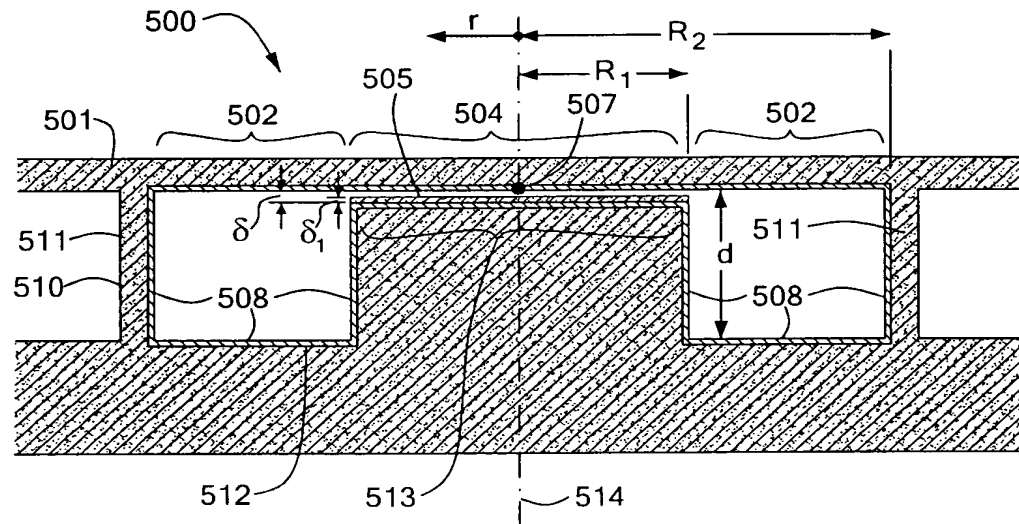
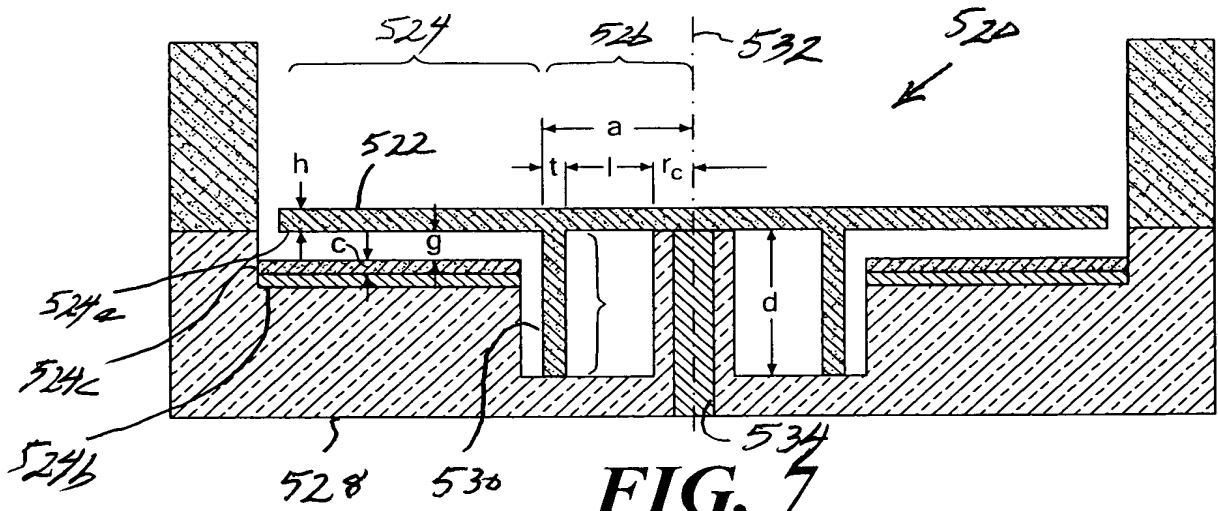


FIG. 5

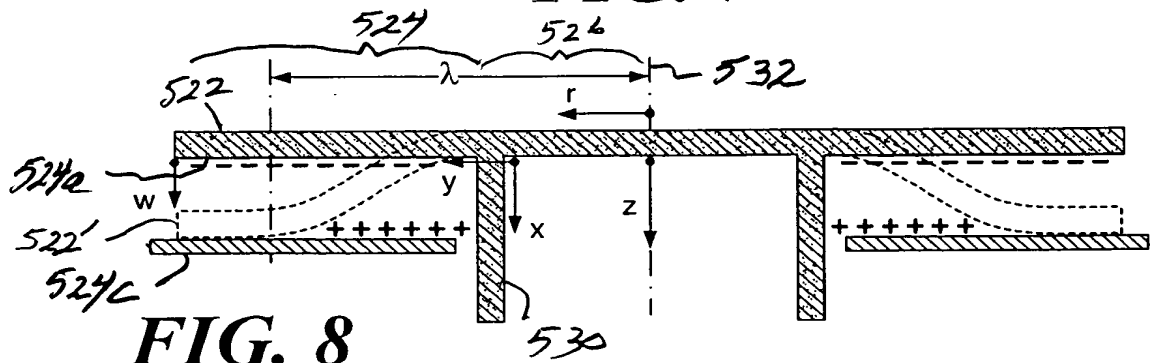
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**FIG. 6**



**FIG.**



**FIG. 8**



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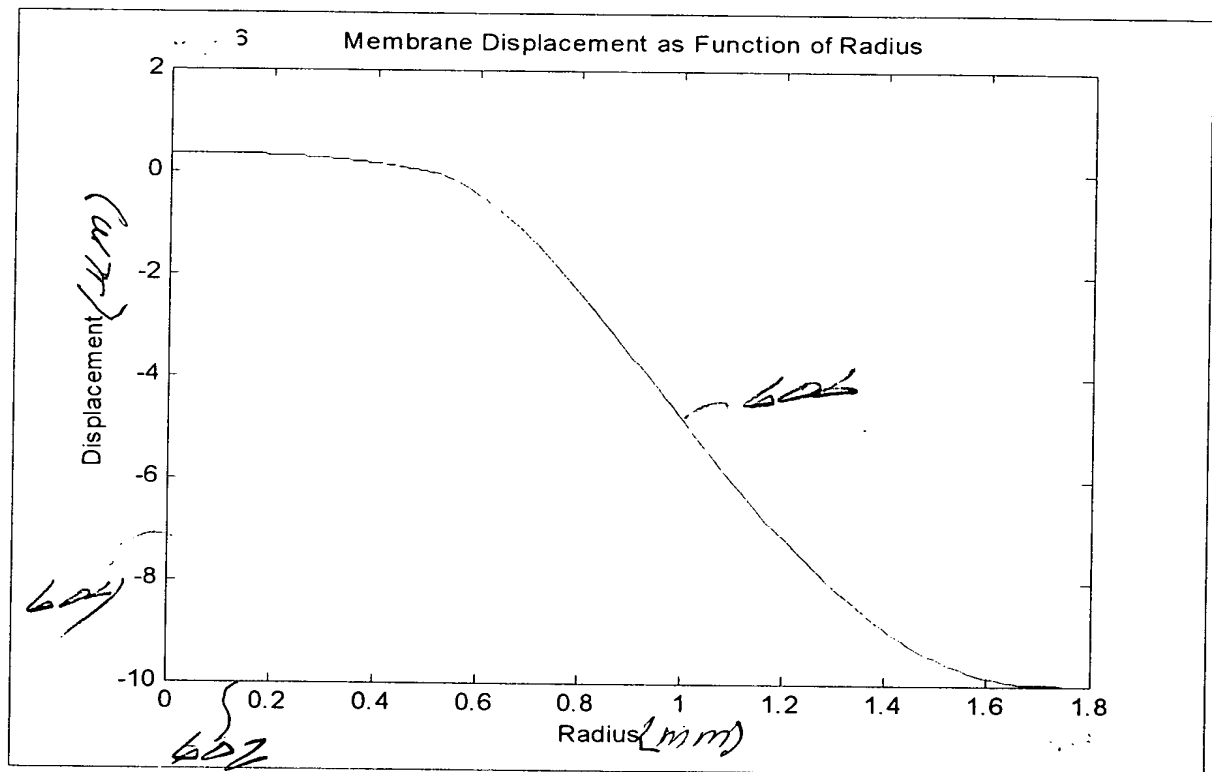


FIG. 9

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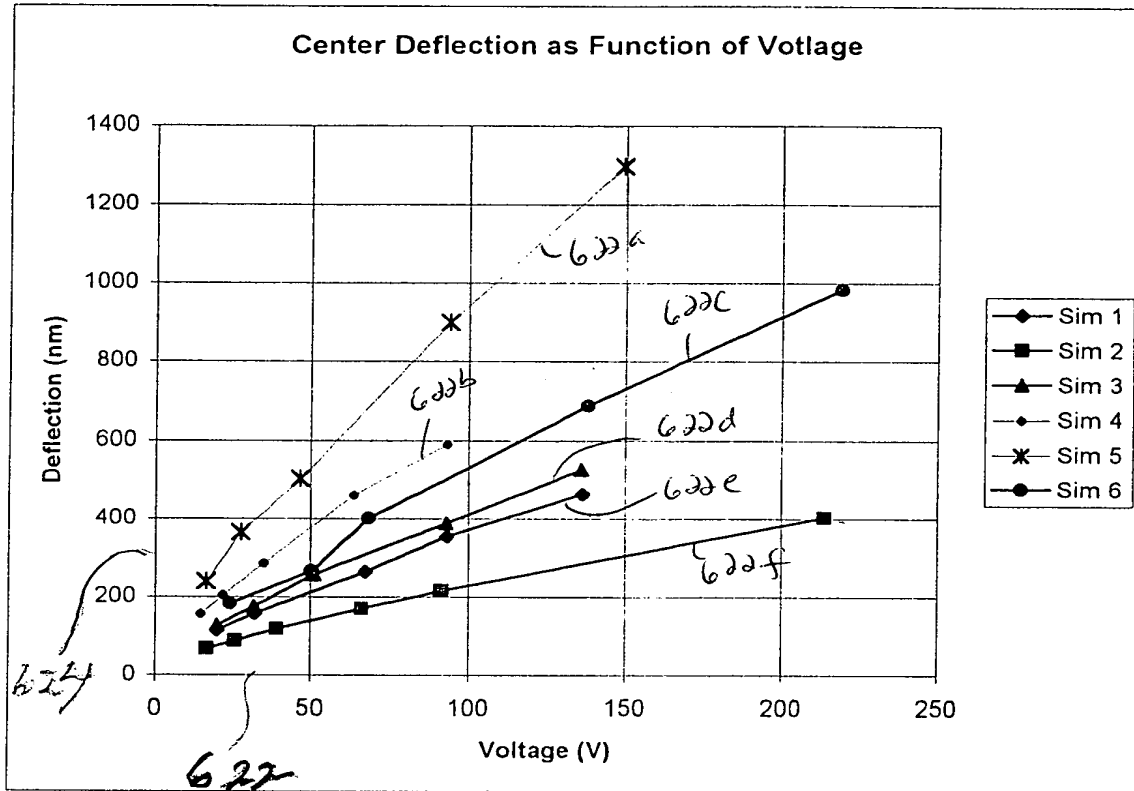


FIG. 10

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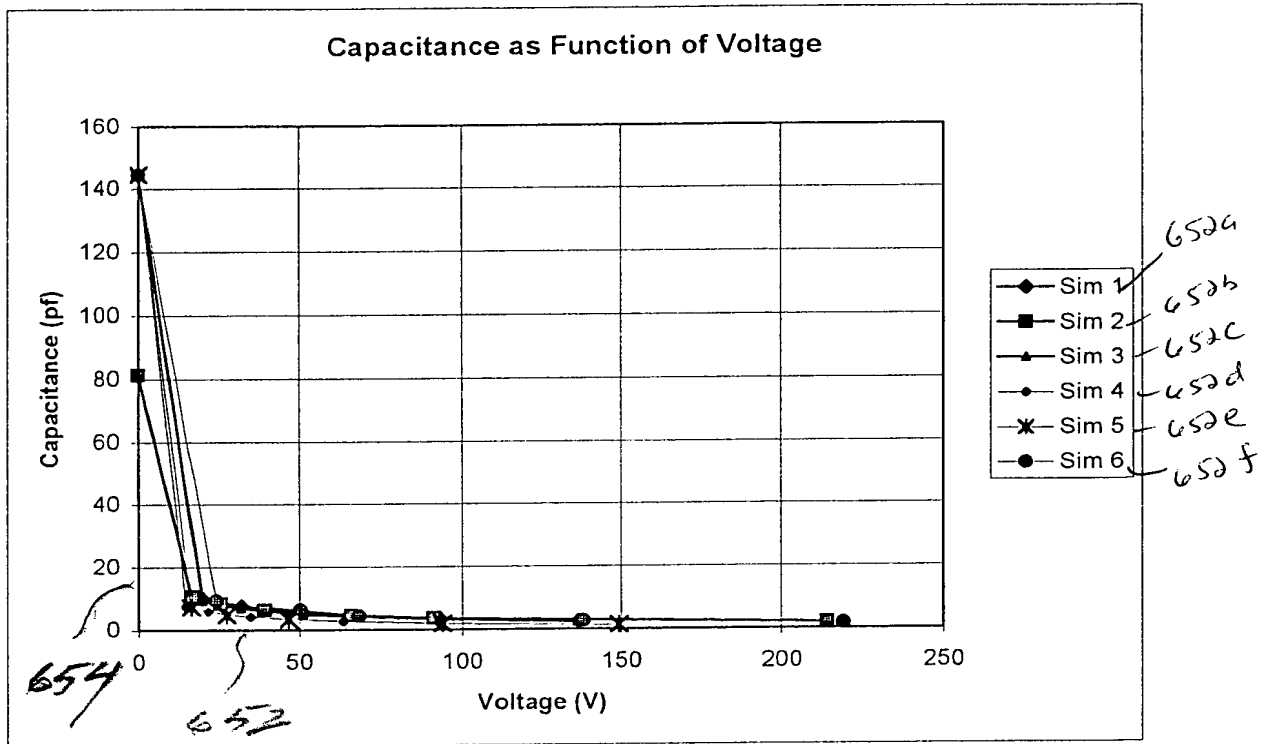


FIG. //

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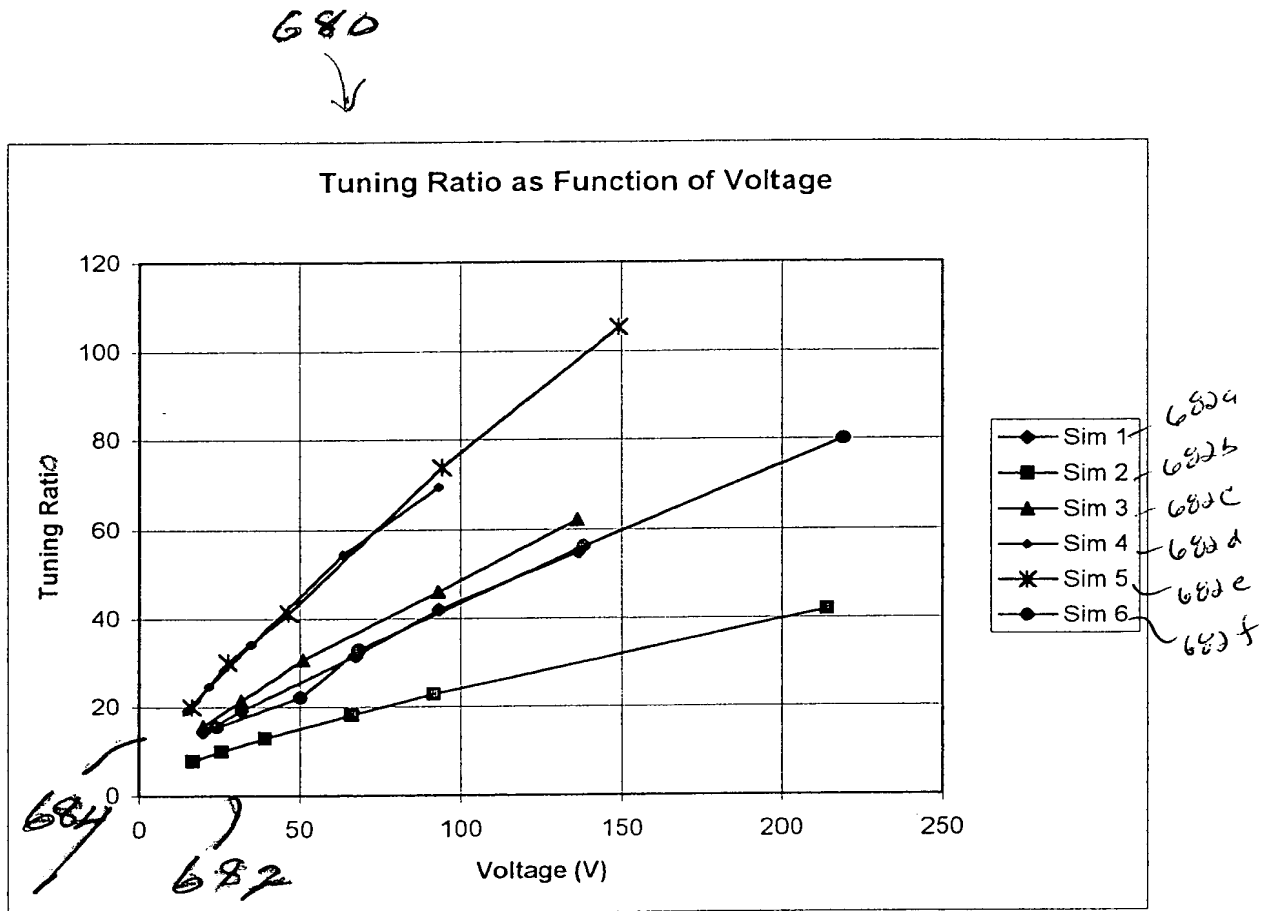
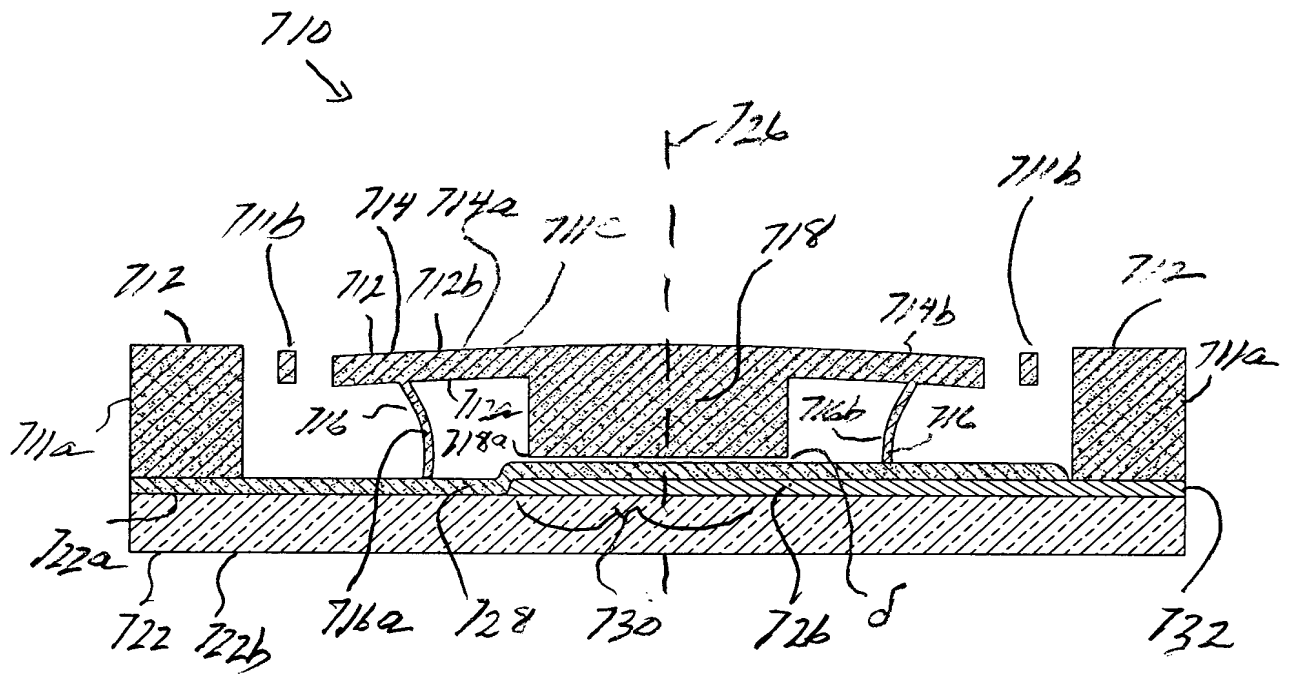


FIG. 12



**FIG. 13**

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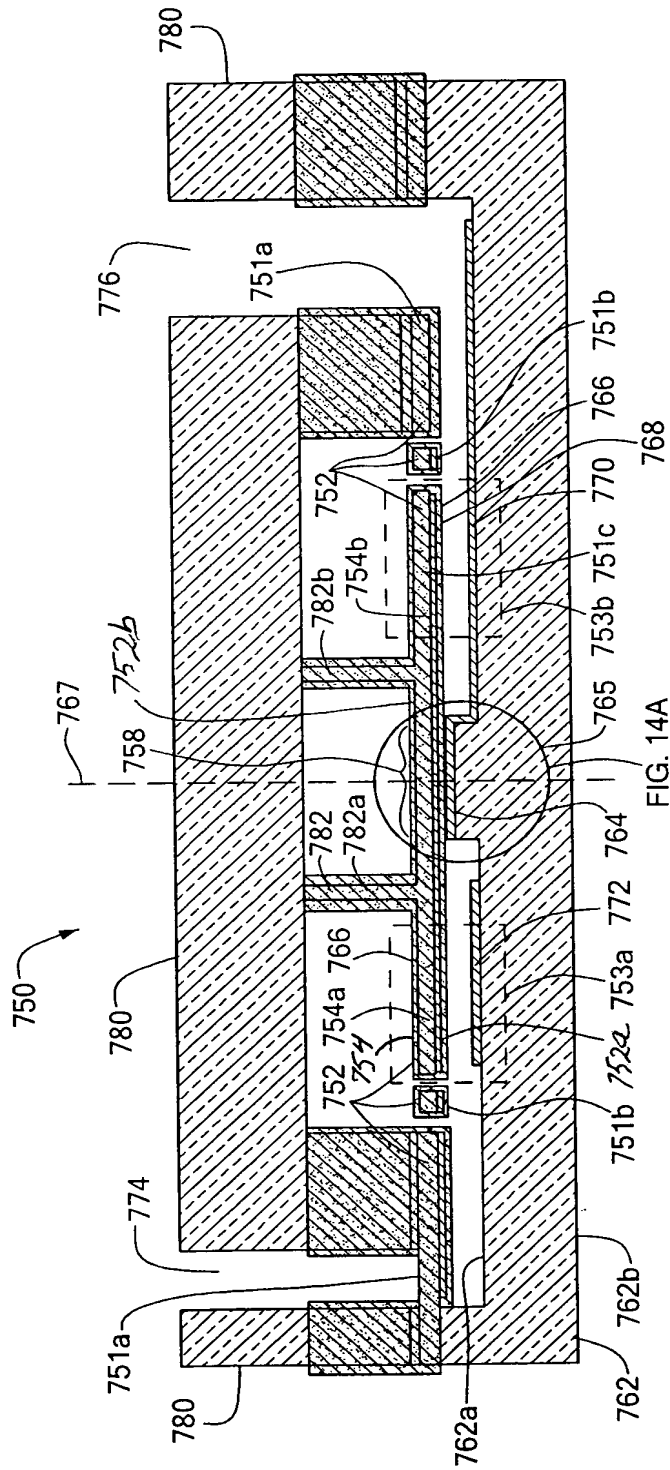
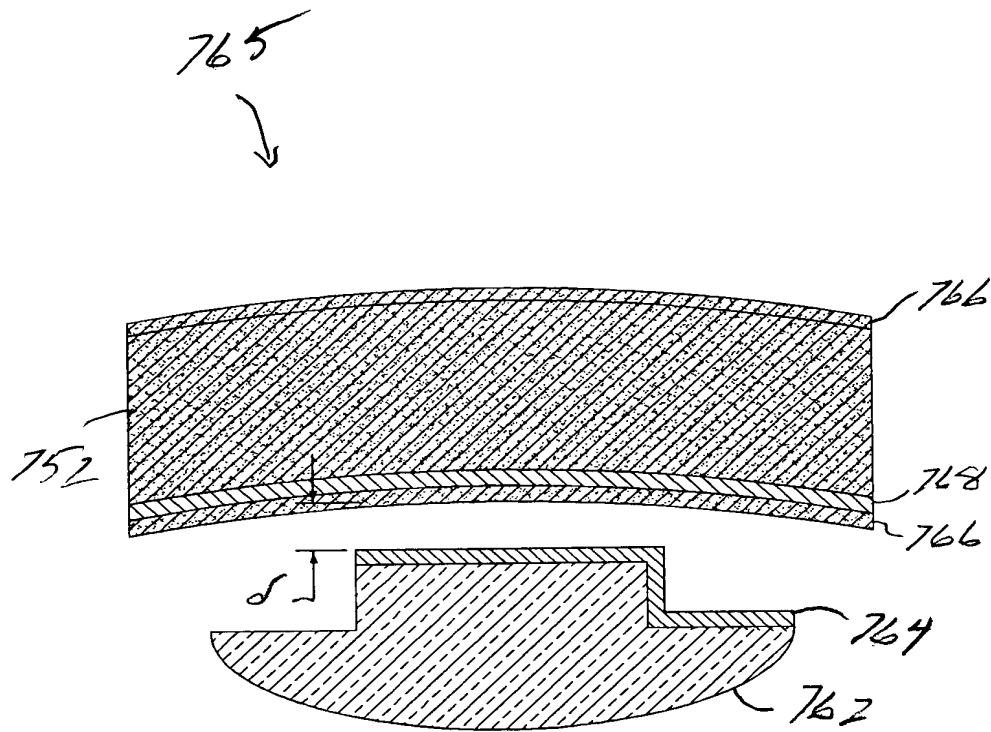


FIG. 14



**FIG. 14A**

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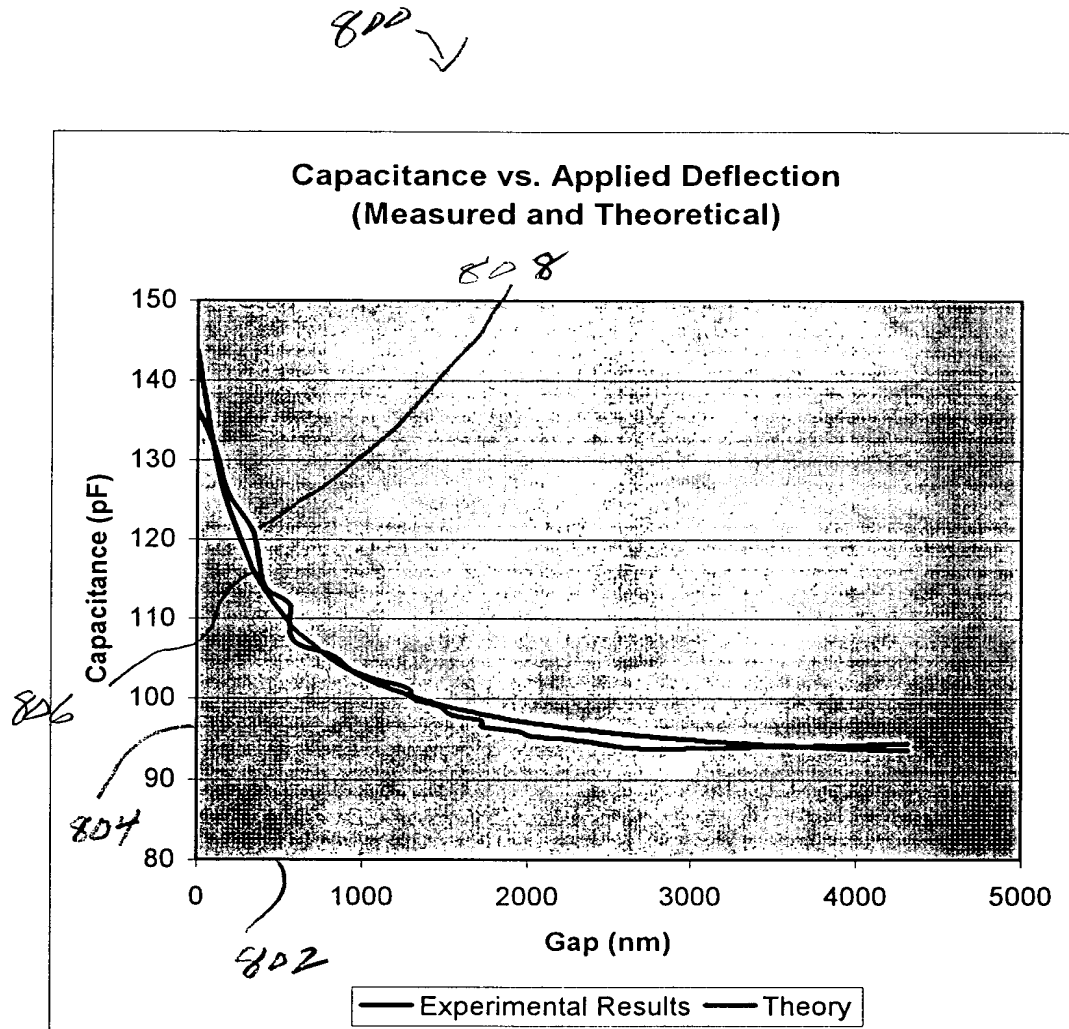


FIG. 15



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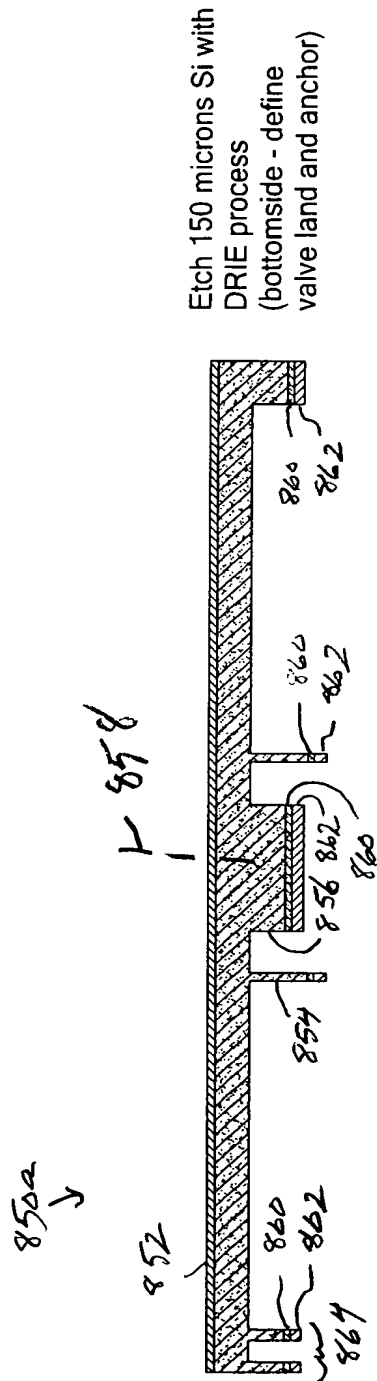


FIG. 16

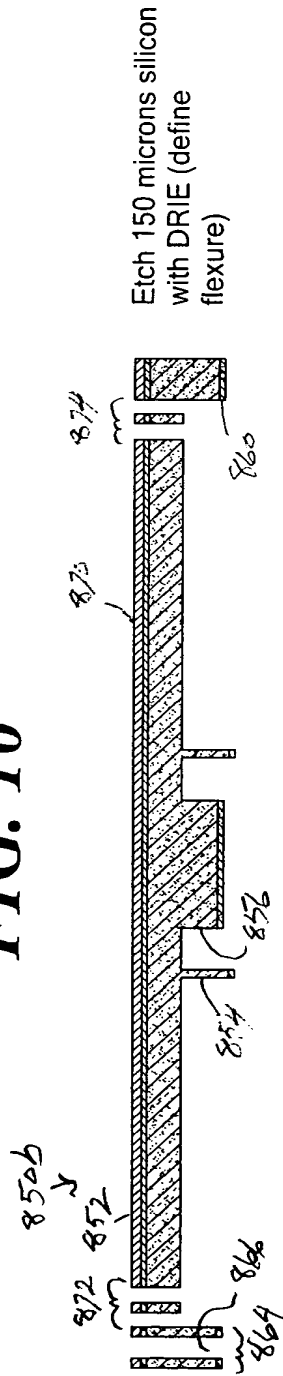


FIG. 16A

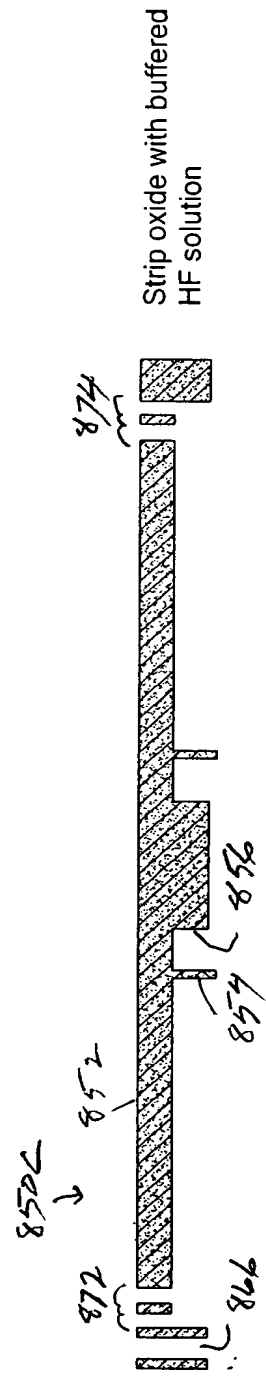


FIG. 16B

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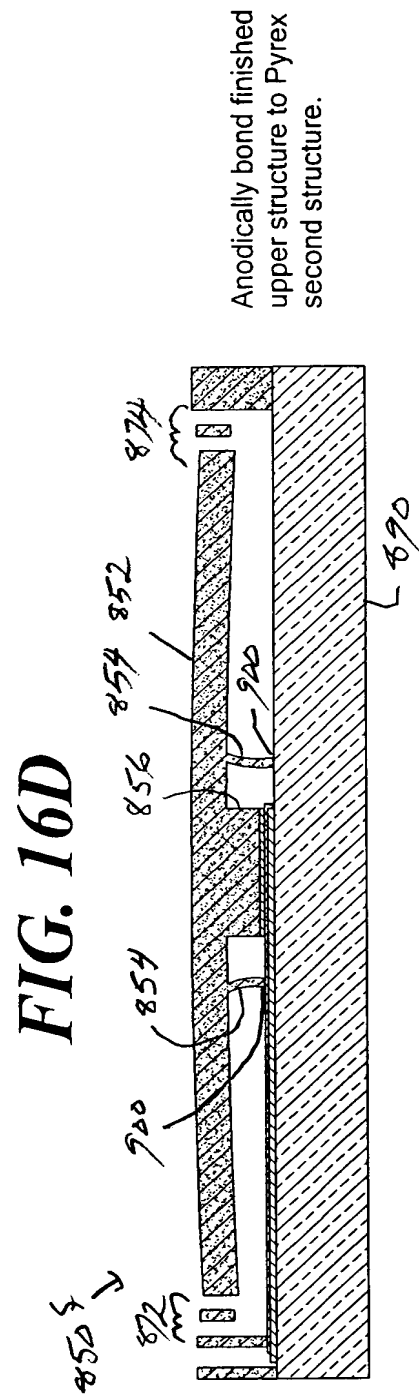
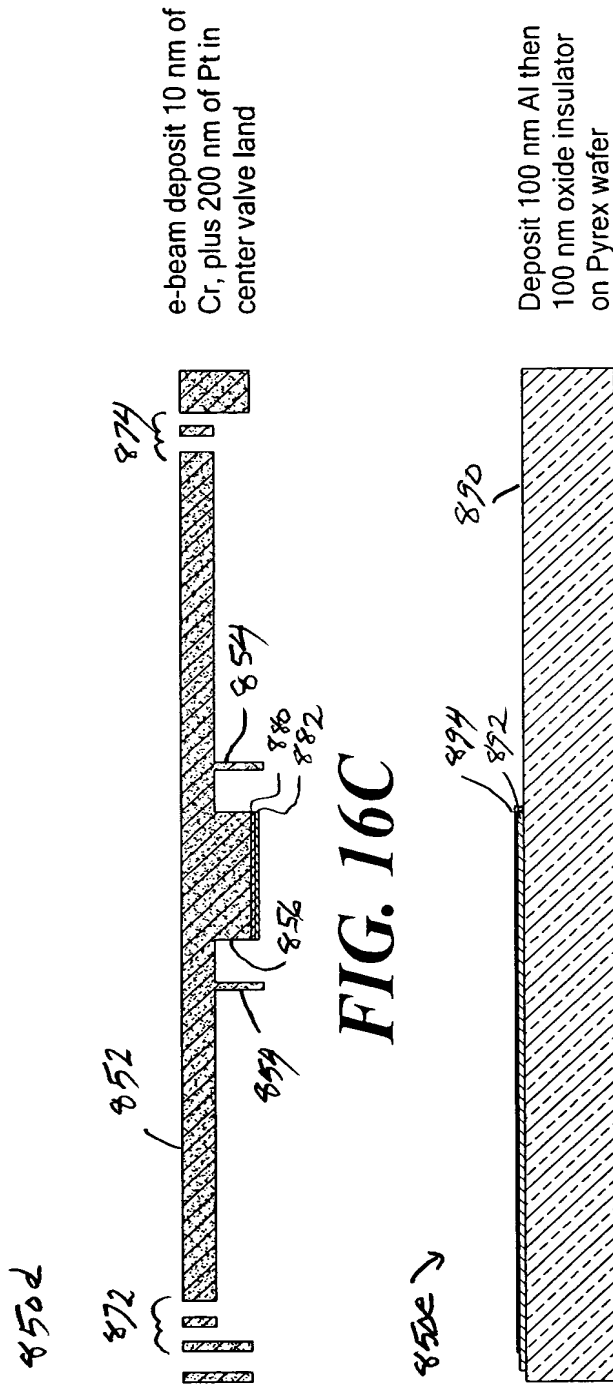
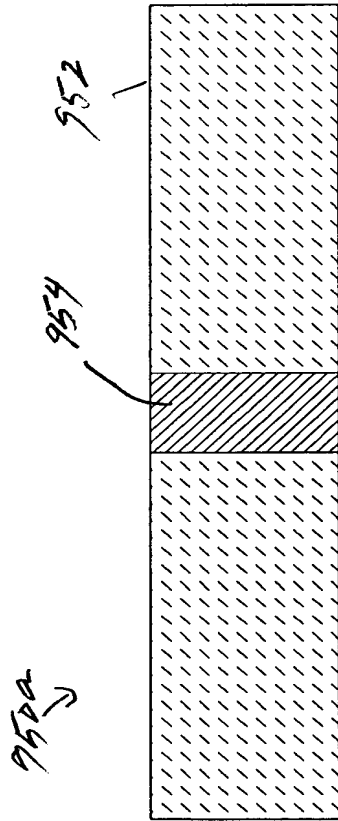


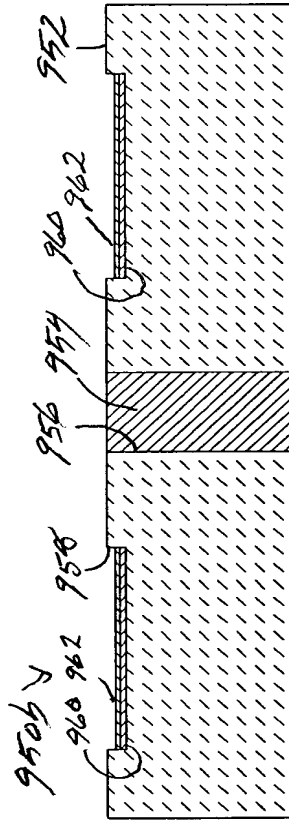
FIG. 16E

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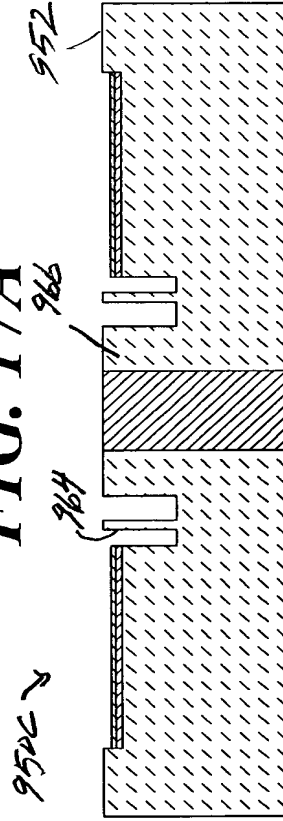
Starting Substrate: Amorphous Quartz  
 500 microns thick  
 Ultrasonically drilled vias, backfilled  
 with gold and CMP polished.

FIG. 17



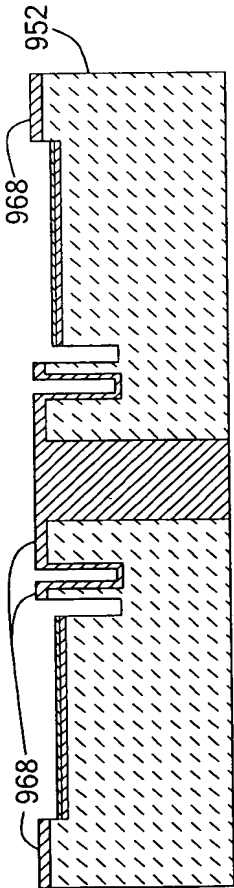
Wet etch shallow cavity (5 microns), deposit  
 metal electrode, then grow low-temperature  
 oxide insulator.

FIG. 17A



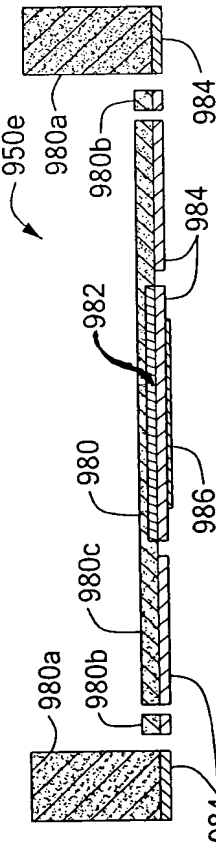
Deep RIE (AOE) etch quartz to define  
 support structure, 100 microns deep.

FIG. 17B



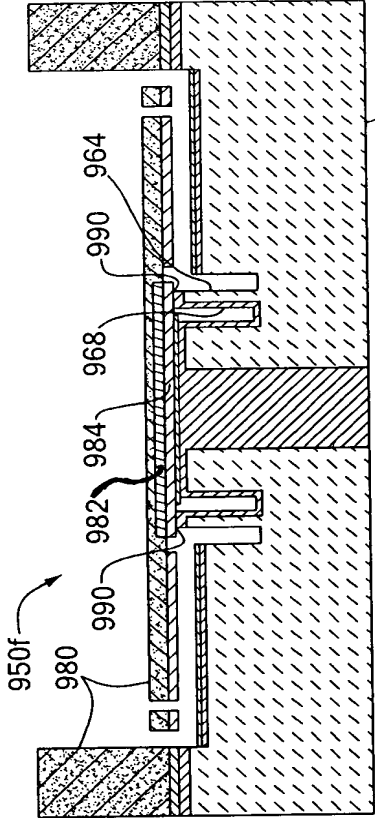
Sputter Ti/Pd seed layer through shadow mask; electroless plate gold metallization. Finished bottom wafer.

FIG. 17C



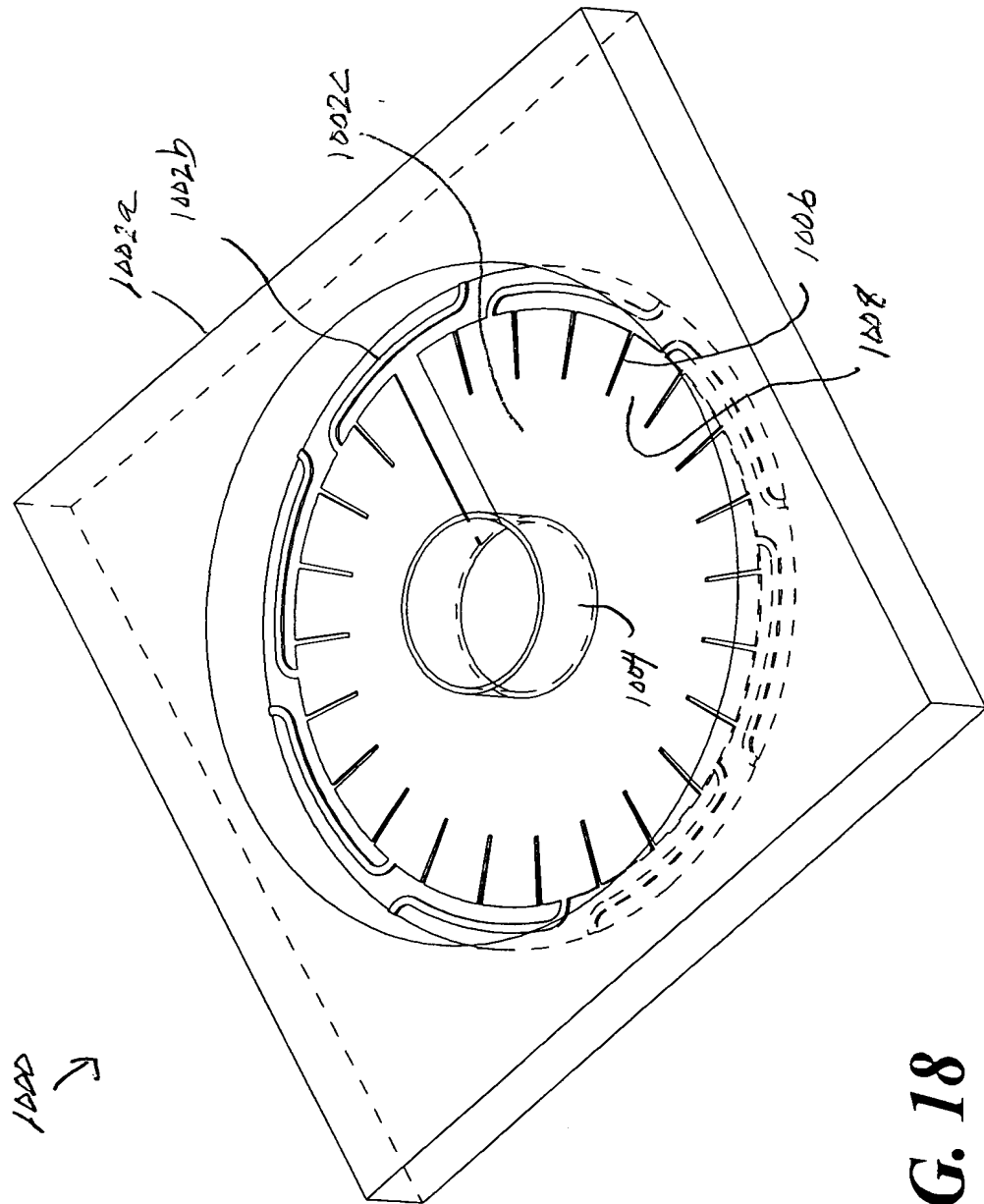
Top Wafer:  
Etch trench and backfill with insulating oxide  
Frontside metallization of diaphragm to define LC tank and actuator regions  
Deposition of thin insulating layer over capacitor region.  
Backside etch to define diaphragm.

FIG. 17D



Thermocompression Au-Au bonding of top flexure and bottom substrate.  
(low-temperature, microwave assisted)  
The insulating layer prevents bonding of the capacitor structure.

FIG. 17E



**FIG. 18**

